SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

AND IMAGING SYSTEM

BACKGROUND OF THE INVENTION

The present invention relates to a noise reduction technique in the imaging system utilizing an imaging element such as a CCD (charge coupled device) and more specifically to a technique for reducing noise generated by transmission of a digital image data with a code conversion system, for example, to a technique which can effectively be adapted to an electronic still camera (so-called a digital camera) and a video camera.

As shown in Fig. 10, there is provided an imaging system such as an electronic still camera or a video camera in which an analog video signal outputted from a CCD 10 is converted into a digital signal in an LSI (large scale semiconductor integrated circuit) for AD conversion 20, this video signal is processed in a DSP (digital signal processor) 30 and the signal is then displayed on a display 80. Here, the CCD 10 and DSP30 are also packed respectively in a semiconductor integrated circuit like the LSI for AD conversion 20 and these semiconductor integrated circuits are mounted on a printed wiring substrate 100 to form an imaging system.

SUMMARY OF THE INVENTION

The inventors of the present invention have investigated in detail the cause of noise appearing on a display image of such imaging system. As a result, the inventors have found the major causes in the events that a power supply noise generated at the time of outputting a video data from the AD conversion LSI 20 in order to transmit the AD-converted video data to the DSP30 migrates into the CCD side via the power supply line (Vcc line and ground line) on the printed wiring substrate and thereafter appears on the video signal to be inputted to the AD conversion LSI and that such power supply noise migrates into the input terminal side from the output circuit side through the power supply and semiconductor substrate within the AD conversion LSI.

Since an output circuit of LSI is requested to drive a load such as external printed wiring which is larger than a load within a chip, an output element used is also large in size (10 times or more) in comparison with the elements forming the internal circuit such as AD conversion circuit and therefore the circuit is usually designed to allow a comparatively large amount of current to flow. Therefore, it is thought that a noise appears on the power supply because a large current flows when an output signal is changed over. Moreover, noise generated in the output circuit is also propagated also to an internal circuit other than the input circuit

via the substrate, but since the AD conversion LSI includes an amplifying circuit such as a PGA (programmable gain amplifier) for amplifying an input analog signal, the noise propagated to the input side is also amplified together with the video signal and thereby display quality may be deteriorated.

Therefore, the same inventors have attempted, in order to reduce noise resulting from operations of the output circuit, connection of a pass-capacitor having a comparatively large capacity to the power supply terminal of the AD conversion LSI as a measure to reduce the noise. However, it has been proved that a large pass-capacitor provided results in increase of a chip size and causes reduction of system loading efficiency and moreover only the pass-capacitor cannot remove the noise sufficiently.

Therefore, the inventors have reached the conclusion that it is very effective for reduction of noise to reduce a through-current in the output circuit resulting from the change-over of the digital video data outputted from the AD conversion LSI 20. It is certainly a measure to reduce the through-current in the output circuit to lower the power supply voltage and lower a driving power of the output circuit. However, in this case, the transmission rate of the signal is lowered and thereby performance of the system can no longer be satisfied.

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Therefore, it is an object of the present invention to provide a semiconductor integrated circuit which can reduce a through-current flowing into an output circuit when an output is changed over and thereby reduces a noise appearing in the output circuit.

The other object of the present invention is to provide an imaging system which can improve image quality by reducing a noise generated in an output circuit which converts an analog video signal outputted from a solid state imaging element such as CCD into the digital video data and then outputs such digital video data without lowering of the transmission rate of the signal.

The aforementioned and other objects and novel features of the present invention will become apparent from the description of this specification and the accompanying drawings.

Outline of the typical inventions disclosed in this specification will be explained as follows.

Namely, the AD-converted digital video data is encoded by the differential encoding method before it is outputted and such encoded signal is then outputted after conversion to the gray code or conversion to the predetermined code through addition of a certain fixed value. In more practical, after the analog color video signal outputted from the imaging element is AD-converted in the AD conversion circuit, a difference

between the codes of the adjacent pixels is obtained in regard to the same color after the AD conversion and the output code of this difference process is then converted into the code with less change-over bits between the adjacent codes. Through such code conversion, the number of bits changing when the output digital signal is changed over is lowered, thereby a through-current in the output circuit is reduced and noise due to change of output can be lowered.

Moreover, the present invention comprises an amplifying circuit for amplifying an analog color video signal outputted from an imaging element, an AD conversion circuit for converting the amplified signal into the digital signal, a differential means for obtaining a difference of the codes of adjacent pixels in regard to the same color after the AC conversion and a code conversion means for code conversion of an output of the differential means. Thereby, the number of bits changing when the digital signal output from the semiconductor integrated circuit is reduced and thereby a through-current in the output circuit can also be reduced.

As the code converting means, it is preferable to use a binary gray code converting circuit for changing the input binary code into the gray code. Thereby, the number of bits which change when the output digital signal is changed over can surely be reduced.

Moreover, as the code converting means, it is also possible to use a circuit for adding a fixed value to the input code or subtracting a fixed value from the input code. Thereby, the number of bits changing when the output digital signal is changed over can be reduced considerably. The reason is based on the following principle. That is, the differential element of the digital video data is concentrated to the data near zero such as 0, +1, -1 or the like. Therefore, the data becomes all "0" in the binary code, but since -1 is all "1", when the differential data changes to -1 from 0 or vice versa, all bits change and thereby noise is generated. Therefore, generation of changes to all "1" from all "0"or vice versa is prevented by adding a fixed value to the input code or subtracting a fixed value from the input code.

Moreover, the differential means explained above is constructed by a delay circuit for delaying an output code of the AD conversion circuit and a subtraction means for obtaining difference between the code delayed with the delay circuit and the input code and the delay circuit for changing the delay time depending on color arrangement of the input video signal. Thereby, even if the color arrangement of the filter used is different, it may be easily covered by changing a delay time of the delay circuit.

Moreover, the imaging system of the present

invention is constructed by an imaging element being provided with a color filter, an amplifying circuit for amplifying an analog color video signal outputted from the imaging element, an AD conversion circuit for converting the amplified signal into a digital signal, a differential means for obtaining a difference between codes of the adjacent pixels in regard to the same color after the AD conversion, a semiconductor integrated circuit being provided with a first code converting means for code conversion of an output of the differential means and a semiconductor integrated circuit for image processing being provided with a second code converting means for converting the code outputted from the semiconductor integrated circuit and an image processing circuit.

According to the means explained above, a through-current in the output circuit of the semiconductor integrated circuit provided with the AC conversion circuit can be reduced, noise resulting from change of output can also be controlled and as a result, display quality can be improved.

It is preferable that the first code conversion means uses a binary gray code conversion circuit for converting a binary code to the gray code, while the second code conversion means uses a gray binary code conversion circuit for converting the gray code to the binary code. Thereby, the number of bits which change

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whenever the output digital signal is changed over can be surely reduced and the display quality can be improved.

Moreover, it is also possible to use a circuit for adding the fixed value to the input code or subtracting the fixed value from the input code as the code conversion means explained above. Accordingly, the number of bits which change when the output digital signal is changed over can be reduced considerably and the display quality can also be improved.

Moreover, the differential means is constructed by a delay circuit for delaying an output code of the AD conversion circuit and a subtraction circuit for obtaining a difference between the code delayed by the delay circuit and the input code, while the delay circuit is constructed to change a delay time depending on the color arrangement of the input video signal. Thereby, even if the color arrangement of the filter used is different, it can be covered easily by changing a delay time of the delay circuit.

Moreover, in the construction of the present invention, a storage means is provided for storing a digital video data, the semiconductor integrated circuit for image processing explained above is provided with a data compression circuit for compressing the code converted by the second code converting means and a data expanding circuit for

expanding the compressed data and the data compressed by the data compression circuit is stored in the storage means explained above. Thereby, many video data can be stored in the storage means of small storing capacity while video data compatibility is assured.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing an example of schematic construction of an AD conversion LSI to be used for the imaging system to which the present invention is adapted.

Fig. 2 is a block diagram showing an example of schematic construction of an encoding & code converting circuit.

Fig. 3 is a block diagram showing an example of construction of a binary gray conversion circuit.

Fig. 4 is a layout diagram showing an example of construction of a filter used for an electronic camera.

Fig. 5 is an explanatory diagram of code conversion showing a practical example of differential encoding and binary gray conversion in the AD conversion circuit of a preferred embodiment.

Figs. 6A and 6B are graphs showing the frequency (number of times) of the number of change-over bits of the video data after the AD conversion in the existing imaging system and the frequency of the number of change-over bits of the video data after the AD

conversion in the system to which the present invention is adapted.

Fig. 7 is a block diagram showing an example of construction of DSP for processing the video data after the AD conversion.

Fig. 8 is a block diagram showing an example of construction of the gray binary difference decoding circuit provided in the DSP.

Fig. 9 is a block diagram showing an example of practical construction of the gray binary conversion circuit.

Fig. 10 is a block diagram showing an example of schematic construction of an ordinary imaging system.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of the present invention will be explained with reference to the accompanying drawings.

Fig. 1 shows an example of the schematic construction of the AD conversion LSI to be used for the imaging system to which the present invention is adapted.

As shown in Fig. 1, the AD conversion LSI 20 of the preferred embodiment is composed of a correlation double sampling circuit (CDS) 21 for sampling an analog video signal which is outputted from a CCD 10 and is then inputted to an input terminal IN, a programmable

gain amplifier (PGA) 22 which can vary the gain for amplifying the sampled signal, an AD conversion circuit (ADC) 23 for converting the amplified analog signal into a digital signal, an encoding & code converting circuit 24 for differentially encoding the AD-converted digital video data and then converting such signal to the gray code and an output buffer 25 for outputting the code-converted signal to the external side of chip from an output terminal OUT.

Of the circuit blocks 21 to 25 forming the AD conversion LSI 20, the other circuits except for the encoding & code converting circuit 24 are also provided in the existing AD conversion LSI 20. Namely, it is the characteristic property of the present invention that the encoding & code converting circuit 24 is provided between the AD conversion circuit 23 and output buffer 25.

The circuits provided in the AD conversion LSI 20 of this embodiment does not mean the all circuits shown in Fig. 1. Although, not illustrated in Fig. 1, in such LSI chip, a control circuit for generating a signal to control the gain of the amplifier (PGA) 22 and controlling total operations of the chip, a clock generation circuit for generating a clock signal to give the sampling timing to the CDS21 and also generating the clock signal required respectively for the operations of the AD conversion circuit 23 and the

encoding & code decoding circuit 24 and a block buffer for distributing the clock signal supplied from the external circuits to the circuits within the chip.

Moreover, in this embodiment, noise can be reduced by reducing a through-current in the output buffer 25 as will be explained later by providing the encoding & code decoding circuit 24, but it is preferable to connect a pass-capacitor to the power supply terminal of the chip in view of further reducing noise. However, since a pass-capacitor having a smaller capacitance value may be used by applying the present invention, the loading area can be reduced.

Fig. 2 shows a schematic construction of the encoding & code decoding circuit 24. As shown in Fig. 2, the encoding & code decoding circuit 24 is composed of a delay circuit 41 for delaying the data outputted from the AC conversion circuit 23 as much as the predetermined clock period, a difference encoding circuit 42 for obtaining a difference between the data outputted from the AD conversion circuit 23 and the data delayed by the delay circuit 41 and a code conversion circuit 43 for converting the differentially encoded binary data into the gray code.

The difference encoding circuit 42 rounds down the carry bit which is formed to round down the carry bit which is generated when a difference is obtained. Thereby, the number of bits of data before a difference

is obtained becomes identical to the number of bits of
data after a difference is obtained and thereby data
can be processed more easily. The Table 1 shows the
result of arithmetic operations when the carry is
rounded down by obtaining a difference between the data
(value a from which the subtraction is carried out) and
the data (subtraction value b) in an example of 2 bits
and the result d (= c + d) to obtain the value a from
which the subtraction is carried out by addition from
the result of calculation c and subtraction value b.
In this embodiment, the carry bit generated is rounded
down even in the addition which is carried out at the
time of difference decoding explained later.
Accordingly, the number of bits of the data before
obtaining a difference becomes identical to the number
of bits of data after obtaining a difference.

Table 1:

Value a	Value b	c (= a − b) Carry round-down	d (= c + b) Carry round-down
0 0	0 0	0 0	0 0
0 0	0 1	1 1	0 0
0 0	1 0	1 0	0 0
0 0	1 1	0 1	0 0
0 1	0 0	0 1	0 1
0 1	0 1	0 0	0 1
0 1	1 0	1 1	0 1
0 1	1 1	1 0	0 1
1 0	0 0	1 0	1 0
1 0	0 1	0 1	1 0
1 0	1 0	0 0	1 0
1 0	1 1	1 1	1 0
1 1	0 0	1 1	1 1
1 1	0 1	1 0	1 1
1 1	1 0	0 1	1 1

11	11	00	11

In the Table 1, the code (a) of the first column is identical to the code (d) of the fourth column. From this fact, it can be understood that the original code can be recovered accurately by executing the round-down of the carry respectively at the time of the difference encoding and difference decoding. An example of the 2-bit code is shown in the Table 1, but reproducibility can be attained even when the carry is rounded down in the same manner even in the code of three or more bits.

The code conversion circuit 43 is constructed, for example, by the exclusive OR gates G1 to G7 in such a number which is smaller by one than the number of bits of the code to be converted, for example, as shown in Fig. 3 and this circuit 43 outputs an exclusive OR of the adjacent bits D_i, D_{i+1} (i = 0 to 6) except for the most significant bit as the bit "Di" after the code conversion. The most significant bit D7 before the code conversion is outputted in direct as the most significant bit D7' after the code conversion. Fig. 3 shows an example of the circuit for conversion example of the binary code of 8 bits to the gray code. Therefore, the code conversion circuit for the desired number of bits such as 10 bits and 12 bits, etc. can be constructed in the same manner.

Next, the practical procedures of the difference

encoding process by the difference encoding circuit 42
and binary gray code conversion by the code conversion
circuit 43 will be explained with reference to Fig. 5.
The procedures explained here correspond to the case
where the video signal outputted from the CCD which
includes a color filter in which the three primary colors
R(red), G(green) and B(blue) are arranged as shown in
Fig. 4(A) and is constructed to sequentially scan each
line shown by the arrow marks □ to □ in Fig. 4(A) from
the upper side in the horizontal direction. In this
case, amount of delay in the delay circuit 41 of Fig.
2 is defined as the amount of delay of two clock periods,
namely two clock periods of the sampling clock of the
input signal in the CDS21.

Here, it is assumed that the signals of R(red) and
G(green) are alternately inputted such as R→G→R→G
→R→G→R→G as indicated in the column (A) of Fig. 5.
In this case, it is also assumed that a value obtained
by AD conversion of each signal is changed to the value
in the column (B) of Fig. 5 in the decimal number. Such
value can be expressed with the binary code which is
actually outputted as shown in the column (C) of Fig.
5. This code has been outputted in direct from the
existing AD conversion LSI not including the encoding
& code converting circuit 24. As will be apparent from
the comparison of the adjacent codes in the column (C)
of Fig. 5, the number of change-over bits when each code

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is changed to the next code can be expressed with the code in the column (D) of Fig. 5.

The values outputted from the difference encoding circuit 42 when the binary code as shown in Fig. 5(C) is inputted to the code conversion circuit 24 of this embodiment can be expressed in the decimal number as shown in Fig. 5(E) or expressed in the binary code as shown in Fig. 5(F). Here, the difference means a difference between the same colors of the adjacent pixels, namely a difference between every other values as shown by the arrow marks in the column (B) of Fig. 5. The difference binary code of Fig. 5(F) can be converted to the gray code as shown in Fig. 5(G).

As will be apparent from comparison between the adjacent codes in the column (G) of Fig. 5, the number of change-over bits when each code is changed to the next code is shown in Fig. 5(H). Comparison between the columns (D) and (H) of Fig. 5 will makes it apparent that the number of change-over bits is remarkably reduced in this embodiment from that of the existing system.

Since distinctive change between the adjacent pixels is small in the video signal, amount of change in the bits of the same colors is also small even when the code after the AD conversion is immediately converted to the gray code. In this embodiment, the code after the AD conversion is not immediately

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converted to the gray code and only a difference is obtained because a code difference between different colors of one pixel in an output of the CCD having passed the filter in the color element arrangement as shown in Fig. 4 is comparatively larger even when change between the adjacent pixels is rather smaller in the video signal (only exception is that difference of codes between different colors is also small in the case of gray color in which the imaging object is poor in change of color).

When the code is converted to the gray code by obtaining a difference as in the case of this embodiment, since there is no such a large difference between the differences even when the color is different, the number of bits is also reduced when an output of the video data of the R(red) element is changed over, for example, to the output of the video data of the G(green) element.

However, if only a difference is obtained, the events in which a difference becomes positive or negative in one display image are assumed to be generated almost in the same rate but the code is changed to a large extent to all "1" from all "0" when the binary code expressed with the 2's complement is changed to negative from positive or to all "0" from all "1" when such binary code is changed to positive from negative. Therefore, in this embodiment, the code does not change to a large extent for change to negative from positive

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or change to positive from negative by converting the binary code tot the gray code.

Table 2 shows an example of the relationship between the binary code expressed with the 2's complement and the gray code when the code is formed of three bits.

Table 2:

Decimal	Binary (2's complement)	Gray code	Offset binary (+5)
7	111	100	100
6	110	101	011
5	101	111	010
4	100	110	001
3	011	010	000
2	010	011	111
1	001	001	110
0	000	000	101
−1(7)	111	100	100
−2(6)	110	101	011
−3(5)	101	111	010
−4(4)	100	110	001
−5(3)	011	010	000
−6(2)	010	011	111
−7(1)	001	001	110

As will be understood from the Table 2, when the decimal number changes to "-1" from "0", the binary code of three bits changes to "111" from "000". Moreover, in the case of the code of 4 bits, 8 bits or more bits, the codes change to all "0" from all "1". In this case, all bits (three bits) are changed over. On the other hand, when the decimal number changes to "-1" from "0", the gray code, for example, of three bits changes to "100" from "000". Therefore, a through-current flowing when an output is changed over with the output

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buffer is also reduced remarkably when the gray code is outputted than that which flows when the binary code is outputted.

Figs. 6(A) and 6(B) show the graphs of the result (A) of search for the number of change-over bits of the code after the AD conversion by the prior art method when a palm of a man is imaged with the CCD and the result (B) of search for the number of change-over bits of the code when the code is converted to the gray code after the difference encoding through application of this embodiment.

From Figs. 6(A) and 6(B), it can be understood that the number of change-over bits in this embodiment is less than that in the prior art method, because the number of bits in the highest appearing frequency is "4" when the number of change-over bits of the code is "8" in maximum in the prior art method, while the number of bits in the highest appearing frequency is "2" when the number of change-over bits is "6" in maximum in this embodiment. As explained above, when the number of change-over bits is small, a through-current flowing into the output buffer can be reduced when such code is outputted and thereby the power supply noise and noise which is propagated through the substrate can also be reduced.

The difference encoding and gray code converting system shown in Fig. 2 can also be adapted to the case

where a complementary color filter in which four colors of Cy (Cyane), Ye (Yellow), Mg (Magenta) and G (Green) are arranged is used and the case where a filter in which the three primary colors of R (Red), G (Green) and B (Blue) are arranged in a horizontal line is used. Even if the complementary color filter is used in above cases, when two kinds of color elements are alternately arranged in the same line, it is enough that amount of delay in the delay circuit 41 is set to the two-clock period as explained above in regard to this embodiment.

On the other hand, when the three-primary-color filter in which three color elements are sequentially and repeatedly arranged in a horizontal line is used, it is enough that the amount of delay in the delay circuit 41 is set to the three-clock period. Since the amount of delay in the delay circuit 41 changes depending on the filter used, it is also possible that the delay circuit 41 of the embodiment shown in Fig. 2 is constructed by a variable delay circuit and a register for designating amount of delay (delay clock period) corresponding to such variable delay circuit in order to change the amount of delay in the delay circuit 41 through update of the preset value of this register.

Next, the second embodiment of the present invention will be explained. In this second embodiment, the code is not converted to the gray code after the difference encoding unlike the first embodiment and a

fixed value expressed with a certain binary code is added (or subtracted) after the difference encoding. The code (hereinafter referred to as the offset binary code) of the case where "5 expressed with the decimal number ("101" in the binary code)" is added as the fixed value after the difference encoding is shown in the right side column of the Table 2.

When "5" is added as the fixed value after the difference encoding from the Table 2, the binary code is changed to "100" from "101" when the decimal number changes to "-1" from "0". Therefore, in this case, only one bit is changed over. However, in the case of this system, since the binary code changes to "000" from "111" when the decimal number changes to "3" from "2", the number of bits to be changed over becomes 3. However, amount of change of the signals between the adjacent pixels enters the range from "-1" to "+2"in a certain input video signal, namely in a certain imaging object (a certain video signal has a small difference of luminosity). In this case, even when the second embodiment is adapted, the number of bits to be changed when an output is changed over can be reduced and noise resulting from the change of output can also be reduced.

In the Table 2, the code is composed of three bits and when the number of bits increases, the range of offset binary code in which the number of bits to be changed when the output data is changed over can be

reduced to 1 or less can be widened by adequately selecting the fixed value to be added. Therefore, even when the code is converted to the offset binary code after the difference encoding, the number of bits to be changed when the output digital signal is changed over can be reduced considerably, although it is not so large as in the case of the first embodiment. Thereby, a through-current in the output circuit can be reduced and noise resulting from change of output can also be reduced.

Fig. 7 shows a schematic construction of a DSP (Digital Signal Processor) 30 which executes the data process by receiving a video data outputted from the AD conversion LSI. The DSP 30 of this second embodiment is composed of a gray binary difference decoding circuit 31 which receives the gray-code converted video data outputted from the AD conversion LSI for reverse conversion thereof to the original binary code and then executes the difference decoding, a video signal processing circuit 32 for executing the video process, for example, color compensation and mixing of video signals to the decoded video data and a compression/ expansion circuit 33 for compressing the decoded video data to store it into an external memory 50 and expanding the video data read from the memory 50. As the memory 50, a non-volatile semiconductor memory such as RAM and a non- volatile memory such as smart media and compact

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flash may be used.

Here, it is also possible that the video data after
the image process is compressed with the
compression/expansion circuit 33 and thereafter the
data is stored in the external memory 50, in place of
compressing the video data before the image process in
the video processing circuit 32. In this embodiment,
the video data processed in the DSP30 is then outputted
to the external DA conversion circuit 60 and is converted
to the analog signal. This analog signal is then
supplied to a display 80 through a filter 70 for the
purpose of display. The DSP30 of Fig. 7 is indicated
by the function block and the actual hardware is
constructed by an arithmetic circuit such as a
multiplier or an adder, a register for holding a data
and a control circuit or the like for operating above
circuits in the predetermined sequence depending on the
process contents.

Fig. 8 shows a construction of the gray binary
difference decoding circuit 31 provided within the DSP
30. This gray binary difference decoding signal 31 is
constructed by a gray binary conversion circuit 311 for
converting the gray code indicated in the third column
in the Table 3, for example, when the data is composed
of three bits, to the binary code indicated in the second
column, a delay circuit 312 for delaying the code signal
as much as the predetermined clock period corresponding

to the delay of the delay circuit 41 shown in Fig. 2
and an adder circuit 313 for generating the difference
decoded data by adding the code delayed by the delay
circuit 312 to the code converted by the gray binary
conversion circuit 311. Here, the adder circuit 313
is constructed to round down the carry generated when
the addition is carried out. Even when the adder is
constructed to conduct the round-down of carry when the
difference decoding is conducted, the original code can
be recovered accurately as explained with reference to
the Table 1.

Fig. 9 shows an example of practical construction
of the gray binary conversion circuit 311. As
illustrated in this figure, the gray binary conversion
circuit 311 is composed of the exclusive OR gates G11
to G17 of the number which is less by one than the number
of bits to be converted. The code can be converted to
the binary code with the exclusive OR of each input bit
Di'except for the most significant bit and the bit
(output of the exclusive OR gate) Di+1 after the
conversion in the significant bit side which is higher
by one level than such input bit. The most significant
bit D7'is outputted in direct as the most significant
bit D7 after the conversion. Fig. 9 shows an example
of the circuit for converting the gray code of 8 bits
to the binary code corresponding to Fig. 3 and the code
conversion circuit of the desired bits such as 10 bits

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and 12 bits can be constructed in the same manner.

Fig. 8 and Fig. 9 show examples of the conversion circuit when the code transmitted is the gray code. When the code transmitted is the offset binary code indicated in the fourth column of the Table 2, the circuit for subtracting (or adding) a fixed value from (or to) the input code is used.

The inventions realized by the inventors have been explained above practically based on the preferred embodiments thereof, but the present invention is not limited to above embodiments and may be changed or modified within the scope not departing from the subject matters described in the claims of the present invention. For example, in above embodiments, conversion to the gray code and conversion to the offset binary code have been described as the examples of code conversion which is executed after the difference encoding, but the code conversion is not limited thereto and any type of code conversion may be introduced when a less number of bits to be changed for change-over of the code indicating a difference are used.

Moreover, in above embodiments, the AD conversion LSI loading the CDS (correlated double sampling circuit) has been explained but the CDS may be omitted and also may be constructed by the other chip. In the embodiments, the AD conversion LSI employed in the imaging system using the CCD has been explained but the

present invention can also be adapted to the AD conversion LSI in the imaging system utilizing the imaging element other than CCD such as CMOS image sensor.

In above explanation, the inventions which are mainly realized by the inventors of the present invention are adapted to the imaging system which is the application field of the background of the present invention. However, the present invention is not limited thereto and may be widely introduced, for example, to the system in which the analog signal is processed after conversion into the digital data such as a recording system to process the audio signal.

The typical effects of the present invention may be briefly explained below.

The image quality can be improved by lowering noise generated in the AD conversion LSI output circuit for converting an analog video signal outputted from an imaging element to a digital video data without reduction of the transfer rate of signals.